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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: **CORONEL ET AL.**

Serial No. **Not Yet Assigned**

Filing Date: **Herewith**

For: **DRAM MEMORY INTEGRATION METHOD**

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EXPRESS MAIL NO: EL747059793US

DATE OF DEPOSIT: January 9, 2002

NAME: Dawn Kimler

SIGNATURE: Dawn Kimler

PRELIMINARY AMENDMENT

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Prior to the calculation of fees and examination of the present application, please enter the amendments and remarks set out below.

In the Claims:

Please cancel Claims 1 to 10.

Please add new Claims 11 to 37.

11. A method for making a dynamic random access memory (DRAM) comprising a plurality of memory cells, each memory cell connected to a bit line and a word line and comprising a storage capacitor and an access transistor, the method comprising:

forming a barrier layer on a substrate, and forming a first dielectric layer on the barrier layer;

removing a portion of the first dielectric layer for

defining a plurality of spaced apart openings therein;

forming a first metal layer on the first dielectric layer and in the plurality of openings;

removing the first metal layer from an upper surface of the first dielectric layer while leaving the first metal layer in the plurality of openings for forming lower electrodes of the respective storage capacitors;

removing an upper portion of the first dielectric layer to create a difference in topography between each lower electrode and the first dielectric layer;

forming a second dielectric layer on each lower electrode;

forming a second conductive layer on the second dielectric layer and on the first dielectric layer to form a continuous upper electrode, with the difference in topography being retained in zones where a portion of the upper electrode is to be removed so that a respective bit line contact can be formed;

forming a third conductive layer on the second conductive layer;

implanting dopants in the third conductive layer corresponding to an upper portion of the zones showing the difference in topography;

removing the third conductive layer corresponding to a lower portion of the zones; and

removing the upper electrodes exposed in the lower portion of the zones, and completely removing a remainder of the third conductive layer, the removal of the upper electrodes being self-aligned with respect to the lower

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electrodes.

12. A method according to Claim 11, further comprising forming a plurality of access transistors in the substrate.

13. A method according to Claim 11, wherein each of the first, second and third dielectric layers comprises silicon oxide.

14. A method according to Claim 11, wherein each of the first, second and third conductive layers comprises polysilicon.

15. A method according to Claim 11, wherein the DRAM comprises an embedded DRAM; and further comprising using a mask so that the dopants are only implanted in the third conductive layer corresponding to the upper portion of the zones.

16. A method according to Claim 11, wherein the first conductive layer forming the lower electrodes comprises hemispherical polysilicon grains.

17. A method according to Claim 11, wherein removing the upper portion of the first dielectric layer is carried out by chemical etching, and a duration of the chemical etching determines a depth of the upper portion of the first dielectric layer being removed.

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18. A method according to Claim 11, wherein the second dielectric layer comprises an oxide layer and a nitride layer on the oxide layer.

19. A method according to Claim 11, wherein the dopants comprise BF_2.

20. A method according to Claim 11, wherein a wet solution comprising at least one of KOH and NH_4OH is used for removing the third conductive layer.

21. A method according to Claim 11, wherein removing the upper electrodes and the remainder of the third conductive layer is performed by a plasma ion etching.

22. A method according to Claim 21, wherein the plasma ion etching is an isotropic plasma ion etching.

23. A method according to Claim 21, wherein the plasma ion etching is an anisotropic plasma ion etching.

24. A method for making a dynamic random access memory (DRAM) comprising a plurality of memory cells, each memory cell connected to a bit line and a word line and comprising a storage capacitor and an access transistor, the method comprising:

forming a plurality of access transistors in a substrate;

forming a first dielectric layer on the substrate;

defining a plurality of spaced apart openings in the first dielectric layer;

forming lower electrodes for the respective storage capacitors in the plurality of spaced apart openings;

removing an upper portion of the first dielectric layer to create a difference in topography between each lower electrode and the first dielectric layer;

forming a second dielectric layer on each lower electrode;

forming a continuous upper electrode for the respective storage capacitors on the first and second dielectric layers, with the difference in topography being retained in zones where a portion of the upper electrode is to be removed so that a respective bit line contact can be formed;

forming a conductive layer on the continuous upper electrode;

implanting dopants in the conductive layer corresponding to an upper portion of the zones showing the difference in topography;

removing the conductive layer corresponding to a lower portion of the zones; and

removing the upper electrodes exposed in the lower portion of the zones, and completely removing a remainder of the conductive layer, the removal of the upper electrodes being self-aligned with respect to the lower electrodes.

25. A method according to Claim 24, wherein the DRAM comprises an embedded DRAM; and further comprising using

a mask so that the dopants are only implanted in the conductive layer corresponding to the upper portion of the zones.

26. A method according to Claim 24, wherein the lower electrodes comprises hemispherical polysilicon grains.

27. A method according to Claim 24, wherein removing the upper portion of the first dielectric layer is carried out by chemical etching, and a duration of the chemical etching determines a depth of the upper portion of the first dielectric layer being removed.

28. A method according to Claim 24, wherein the second dielectric layer comprises an oxide layer and a nitride layer on the oxide layer.

29. A method according to Claim 24, wherein a wet solution comprising at least one of KOH and NH_4OH is used for removing the conductive layer.

30. A method according to Claim 24, wherein removing the upper electrodes and the remainder of the conductive layer is performed by a plasma ion etching.

31. A method for making a dynamic random access memory (DRAM) comprising a plurality of memory cells, each memory cell connected to a bit line and a word line and comprising a storage capacitor and an access transistor, the

method comprising:

forming a plurality of access transistors in a substrate;

forming a first dielectric layer on the substrate;

defining a plurality of spaced apart openings in the first dielectric layer;

forming lower electrodes for the respective storage capacitors in the plurality of spaced apart openings;

removing an upper portion of the first dielectric layer to create a difference in topography between each lower electrode and the first dielectric layer;

forming a second dielectric layer on each lower electrode;

forming a continuous upper electrode for the respective storage capacitors on the first and second dielectric layers, with the difference in topography being retained in zones where a portion of the upper electrode is to be removed so that a respective bit line contact can be formed; and

removing the upper electrodes exposed in a lower portion of the zones, the removal of the upper electrodes being self-aligned with respect to the lower electrodes.

32. A method according to Claim 31, wherein before the upper electrodes exposed in lower portion of the zones are removed, further comprising:

forming a conductive layer on the continuous upper electrode;

implanting dopants in the conductive layer

corresponding to an upper portion of the zones showing the difference in topography;

removing the conductive layer corresponding to a lower portion of the zones, and then removing the upper electrodes exposed in the lower portion of the zones along with completely removing a remainder of the conductive layer.

33. A method according to Claim 31, wherein the lower electrodes comprises hemispherical polysilicon grains.

34. A method according to Claim 31, wherein removing the upper portion of the first dielectric layer is carried out by chemical etching, and a duration of the chemical etching determines a depth of the upper portion of the first dielectric layer being removed.

35. A method according to Claim 31, wherein the second dielectric layer comprises an oxide layer and a nitride layer on the oxide layer.

36. A method according to Claim 31, wherein a wet solution comprising at least one of KOH and NH_4OH is used for removing the conductive layer.

37. A method according to Claim 31, wherein removing the upper electrodes and the remainder of the conductive layer is performed by a plasma ion etching.

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REMARKS

It is believed that all of the claims are patentable over the prior art. For better readability and the Examiner=s convenience, the newly submitted claims differ from the translated counterpart claims which are being canceled. The newly submitted claims do not represent changes or amendments that narrow the claim scope for any reason related to the statutory requirements for patentability. Accordingly, after the Examiner completes a thorough examination and finds the claims patentable, a Notice of Allowance is respectfully requested in due course. Should the Examiner determine any minor informalities that need to be addressed, he is encouraged to contact the undersigned attorney at the telephone number below.

Respectfully submitted,

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